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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,427	07/13/2004	Johannes Hubertus Antonius Brekelmans	NL 020021	9429

24737 7590 05/05/2006

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/501,427	Applicant(s) BREKELMANS ET AL.	
	Examiner Thomas J. Hiltunen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7 and 8* is/are rejected.

7)☒ Claim(s) *3-6 and 9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of changes in this action

1. Applicant's amendment has overcome the rejections of claims 1-6 under 35 U.S.C. § 112, second paragraph.
2. Applicant's amendment and remarks have overcome the objections to the drawings

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Weekes et al. (USPN 3,582,802).

With respect to claim 1, Weekes et al. (USPN 3,582,802) discloses in Fig. 2, a differential inverter comprising a differential inverter (49, and input transistors 44, 46, transistors 44, and 46 invert the signals input to them (i.e. they are n-type bipolar transistors, thus when the input signal is above the threshold voltage 44, and 46 will output a low voltage)

- a differential input for receiving a first vector of signals comprising a first input signal (signal input to the control gate of 44) and a second input signal (signal input to

the control gate of 46)

- a differential control input for receiving a second vector of input signals comprising a first control signal (the emitter of 44 receives a bias signal from 48 through resistor 38) and a second control signal (the emitter of 46 receives a bias signal from 48 through resistor 40),

- a differential output for transmitting a third vector of differential signals comprising a first output signal (signal at node 16) and a second output signal (signal at node 18)

- said differential inverter being characterized in that it further comprises a controlled bias generator (48 is controlled by the voltage divided signal) generating the second vector of input signals in response to a bias control signal (it can be seen that 48 generates the bias signals of 44 and 46 (at the node connected to 38 40 and the output of 48, two bias voltages are produced. One biasing the emitter of 44 and the other biasing the emitter of 46), at the node between resistors 38 and 40) which is generated at an output of a voltage divider coupled to the differential output of the differential inverter (Resistors 28 and 30 create a voltage divider, which creates a bias signal at node 26 that is input to 48. It can be seen that the bias signal is created from the first and second output voltages, because the voltage divider is connected to nodes 16 and 18.) said bias control signal being indicative of a DC voltage of the of the differential output (A DC signal will be present between at node 16 and 18. This DC voltage will be input to 48 at node 26. Thus, the bias control will be indicative of a DC voltage.).

With respect to claim 2, it can be seen that resistors 28 and 30 are connected together at node 26, and that 28 is connected to the first output and 18 is connected to

the second output. Also, node 26 outputs a bias signal to bias generator 48. Weekes et al. discloses that the resistance of 28 and 30 is Ra and Rb respectively. Thus, Weekes et al. discloses that the resistance of 28 and 30 can be any reasonable value, which includes values that are equal.

With respect to claims 7 and 8 it can be seen that newly recited claims 7-8 have no patentable distinction between that of claims 1-2 (see section titled "REMARKS/DISCUSSION OF ISSUES" on page 7 of applicant's response filed 03 March 2006, "Unless indicated otherwise, claims are amended for non-statutory reasons: to correct one or more informalities, remove figure label numbers, and/or to replace European-style claim phraseology with American-style claim language."), and thus claims 7-8 rejected for the same reasons are 1-2.

Allowable Subject Matter

Claims 3-6 and 9-12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to claim 3, there was no prior art found that disclosed a differential inverter that has a bias control signal input to a PMOS transistor through a resistive means, and second bias signal input to a NMOS transistor through another resistive means. Yin (USPN 5,705,946) disclosed a level-shifting device in Fig. 4 that has two differential inverters that receive input and bias signals. However, there is no motivation to use a level-shifting device for differential inverter 49. There was no cited prior art that

taught motivation for replacing Weekes et al.'s generic differential inverter 49, with Yin's level shifter. There was also no other prior art found that disclosed the recited language of claim 3, and provided motivation to use it in a circuit that taught the recited language of claim 1. Thus claim 3 is allowable.

With respect to claim 4, There was prior art found that taught the using inverters to split a single input signal into two. However, there was no motivation provided by Weekes et al. to use the signal splitter in its bias circuit. For example Fig. 6 of Yamamoto et al. taught the using an inverter 38b to split a signal to two other inverters (40a and 40b), which are then input to a p and n type transistors 42 and 44. However, there is no motivation to use this type of buffer in place of that of buffer 48 in Weekes et al.. This is because 48 outputs a single signal which is split between two resistors, whereas Yamamoto et al. outputs two signals that are already split. There would be no motivation for adding more circuit components to Weekes et al., because it would be more expensive to manufacture and it would perform the same as the single buffer 48. Chiu et al (USPN 6,734,700) discloses the same situation as Yamamoto et al. in Fig. 1A, and it too doesn't supply any motivation to replace 48 of Weekes et al. with it. Additionally, Tang et al. (USPN 6,794,900) discloses a circuit that has two separate signals that are inverted being supplied to a differential input from the output through a two bias generators. However, these signals are not derived from a single bias signal, which is voltage divided at the between the outputs. Rather, they are derived straight from each differential output. There is no motivation to voltage divide these signals to be input to a bias control. Therefore there would be no single bias signal to be sent to

the signals splitters of Chiu et al. and Yamamoto et al. Thus, claim 4 is allowable, and claim 5 is allowable based on it dependency to claim 4.

With respect to claim 6, there was no prior art found that taught a differential amplifier with an "LC tank" coupled to its outputs and then feedback to the inputs of the differential inverter. There was prior art found that did have a differential inverter with an LC tank between its outputs, such as Fig. 1 of Smith et al. (USPN 6,043,710), Fig. 6 of Horiguchi et al (USPN 5,952,856), and Fig. 9 of Sugawara (USPN 5,495,194). Also, there was no prior art found that provided motivation for combining claim the teachings of Weekes et al. with the any of the cited prior art with LC tanks. No cited prior taught the further recitation a differential inverter having its outputs connected to a LC and cross-coupled to the input of the inverter. Thus, claim 6 is allowable.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Upon an updated search the reference of Shin et al. (USPN 5,703,532) was found, in which it clearly can be seen that Fig 2 of Shin et al. discloses the recited language of claims 1-2, and 7-8, in that Shin et al. discloses a differential inverter (21-22 and 41-42), a controlled bias generator (23-26, and 43-46), which is controlled by two bias voltages (one on gates of 23-26, and the other on the gates of 43-46) derived from a resistive divider (71 and 72), connected to the output voltages (voltage at drains of 24 and 25, and voltage at drain of 44 and 45). Also, the resistive divider is composed of two matched resistors (72 and 71). With respect to claim 3 Shin et al does disclose

CMOS differential inverters composed of NMOS and PMOS circuitry, additionally it can be seen that the bias control circuit is composed of resistors (see Fig. 6). However, it would not be reasonable to consider the drains of 21-22, and the drains of 41-42 as the control input of the differential inverter as required by the recited claim language. Thus, claims 3-6, and 9-12 would be allowable over Shin et al.

Response to Arguments

Applicant's arguments filed 03 March 2006 have been fully considered but they are not persuasive. With respect to the argument that Weekes et al. not disclosing a differential inverter, Examiner finds Applicant's arguments unpersuasive. The broadest reasonable interpretation of a "differential inverter" is a circuit that inverts differential signals. It would be understood by one of ordinary skill in the art would that transistors 44 and 46 are n-type bipolar transistors. First it is clear from the arrow of 44, and 46, which corresponds to the emitter of a bipolar transistor, which would indicate the emitter of an n-type transistor (due to the fact the emitter is pointing away from 44 and 46). Secondly it can be seen Fig. 4 that bipolar transistors are used in Weekes et al.'s circuit. Third regardless of the transistor type a pnp transistor would still output a signal that is inverted with respect to the control signal. It is clear that the Weekes et al. discloses differential signals being used in the disclosed circuit (See, title DIRECT COUPLED DIFFERENTIAL TRANSISTOR.....", line 1 of the abstract discloses "A direct coupled multistage differential amplifier.....".) Thus it would be clear to one of ordinary skill in the art that Weekes et al., discloses differential inputs (and outputs) in the circuit of Fig.

2, and in the broadest reasonable interpretation of 44 and 46 with 49 (49 amplifies the outputs of 44 and 46 and outputs differential signals to nodes 16 and 18) differential inverter.

With respect to the argument that Weekes et al does not disclose a controlled bias generator, Examiner finds Applicant's arguments unpersuasive. Clearly it can be seen that 48 receives the output of 49 (and thus 44 and 46) at node 26, and outputs a bias signal at the first terminals of 38 and 40. A bias voltage is a voltage that controls the output of a transistor (or any other circuit component for that matter) to a certain voltage level (a voltage that is biased to a desired level). It would be understood by one of ordinary skill in the art that 48 outputs a voltage (based on the voltage present at node 26) to the first terminals of 38 and 40, this voltage is then supplied as two different bias voltages through 38 and 40, in which the 38 and 40 control the amount of voltage present at the emitters of 44 and 46 (based on signal output by 48). Thus when the signals input to 44 and 46 become greater than their respective threshold voltages, 44 and 46 will output a voltages that correspond to the bias voltages output to their emitters by 48. Thus clearly 48 is a controlled bias generator, because it generates bias voltages at the emitters of 44 and 46, which are based on value present at node 26.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner
Art Unit 2816

TH
May 1, 2006